IN THE CLAIMS

Please amend the claims as follows.

For the Examiner's convenience, a list of all claims is included below.

1. (Currently Amended) A computer-implemented method comprising:

measuring first electrical characteristics of an interconnection, including generating a first graphical representation of an output of interconnection that is based, at least in part, on the first electrical characteristics; and

determining a test network having second electrical characteristics that include resistive and capacitive values such that the first electrical characteristics of the interconnection are approximated by the ~~second electrical characteristics~~resistive and capacitive values of the test network within a specified tolerance, wherein determining the test network includes adjusting the ~~second characteristics~~resistive and capacitive values based on the first graphical representation, wherein the determining includes creating a second graphical representation of an output of the test network based on the resistive and capacitive values that approximates the first graphical representation of the output of the interconnection within a specified tolerance.

2. (Original) The method of claim 1 wherein the test network is a resistive/capacitive network.

3. (Canceled).

4. (Canceled)

5. (Previously Presented) The method of claim 1 wherein the specified tolerance is 10%.

6. (Original) The method of claim 1 wherein the test network is a resistive network.

7. (Original) The method of claim 1 wherein the test network is a capacitive network.

8. (Original) The method of claim 1 wherein the test network is comprised of a plurality of resistive/capacitive networks.

9. (Original) The method of claim 2 further including:

connecting the resistive/capacitive network between a driver of a first input/output circuit and a receiver of a second input/output circuit.

10. (Original) The method of claim 2 further including:

connecting the resistive/capacitive network between a driver of an input/output circuit and a receiver of the input/output circuit.

11. (Original) The method of claim 10 wherein the resistance and capacitance of the resistive/capacitive network are adjustable.

12. (Original) The method of claim 11 wherein the resistive/capacitive network is implemented on an integrated circuit chip.

13. (Previously Presented) The method of claim 12 wherein the capacitance is distributed gate capacitance.

14. (Original) The method of claim 11 wherein the resistive/capacitive network is implemented on a printed circuit board.

15. (Currently Amended) An apparatus comprising:

an integrated circuit having at least one input/output ports, the at least one input/output ports having a driver and a receiver; and

a test network having second electrical characteristics that include resistive and capacitive values, the test network electrically coupling the driver and the receiver such that an input/output interface interconnection having first electrical characteristics may be emulated therewith, wherein the ~~second electrical characteristics~~resistive and capacitive values are adjusted based on a first graphical representation of an output of the input/output interface interconnection that is generated based, at least in part, on the first electrical characteristics, wherein an output of the test network generates a second graphical representation based on the resistive and capacitive values that approximates the first graphical representation of the output of the input/output interface interconnection.

16. (Original) The apparatus of claim 15 wherein the test network is a resistive/capacitive network.

17. (Original) The apparatus of claim 15 wherein the test network is a resistive network.

18. (Original) The apparatus of claim 15 wherein the test network is a capacitive network.

19. (Original) The apparatus of claim 16 wherein the resistance and capacitance of the resistive/capacitive network are adjustable.

20. (Original) The apparatus of claim 16 wherein the integrated circuit and the resistive/capacitive network are implemented on a same integrated circuit chip.

21. (Original) The apparatus of claim 16 wherein the resistive/capacitive network is implemented on a printed circuit board.

22. (Original) The apparatus of claim 15 wherein the integrated circuit is part of a microprocessor.

23. (Currently Amended) An apparatus comprising:

a test network for an input/output interface having elements selected such that second electrical characteristics of the test network that include resistive and capacitive values

approximate first electrical characteristics of an input/output interface interconnection within a specified tolerance, wherein the ~~second electrical characteristics~~resistive and capacitive values are adjusted based on a first graphical representation of an output of interconnection that is generated based, at least in part, on the first electrical characteristics, wherein an output of the test network generates a second graphical representation based on the resistive and capacitive values that approximates the first graphical representation of the output of the input/output interface interconnection.

24. (Original) The apparatus of claim 23 wherein the elements are resistive elements and capacitive elements.

25. (Previously Presented) The apparatus of claim 24 wherein the resistive elements and the capacitive elements are adjustable such that the test network may be used to approximate the first electrical characteristics of a plurality of input/output interface interconnections.

26. (Original) The apparatus of claim 24 wherein the test network is comprised of a plurality of resistive/capacitive networks.

27. (Original) The apparatus of claim 26 wherein the capacitive elements are distributed RC ladder.

28. (Original) The apparatus of claim 27 implemented within an integrated circuit chip.

29. (Original) The apparatus of claim 27 implemented on a printed circuit board.

30. (Previously Presented) The apparatus of claim 23 wherein the elements are determined such that a second graphical representation of an output of the test network approximates, within a specified tolerance, the first graphical representation of the output of a particular input/output interface interconnection.